EE/CprE/Se 491 Weekly Report 4
10/3/24 - 10/10/24
sdmay25-28
Digital ASIC fabrication
Client & Advisor: Dr. Duwe

Team Members

Calvin Smith – Issue Tracking
Camden Fergen - Testing Lead
John - Team organizer
Nicholas - Verilog Lead
Levi - Client interaction

Weekly Summary

This week we investigated rocketchip and chipyard. We were also able to get VMs set up for us to use, it will make working on the project much easier as we don't have to worry about having environments and how they affect our project.

Pask Week Accomplishments

- Calvin:
    - Progress with rocket chip installation and compilation
    - Compiled sample piece of chisel to verilog code
    - Learned vivado software to a point where I feel reasonably confident with chip testing
    - Created some tcl scripts
- Camden:
    - Contacted ETG to see if we can get a VM up for our chip development
    - Started to configure VM and determine necessary requirements
    - Clarified that licensed software is able to be installed on VM
    - Looked into open-source RISC-V processors to see what is all out there
- John:
    - Looked into FPGA Fabrics and how to design them
    - Worked on some stuff for caravel and Efabless
    - Researched RISC-V processors and eINK displays
    - Worked on presentations
- Levi:
    - Worked on presentations
    - Finished Efabless tutorials

    - Hardened lab1
- Nicholas:
    - Wrote and ran RTL tests for datapath one.
    - Started looking into possible open-source RISC-V Processors.
    - Continued working on using OpenRAM to generate SRAM for datapath two.

Name	Individual Contribution	Hours this Week	Hours Cumulative
Calvin	• Continued trying to debug my local installation of rocketchip • Familiarized myself with vivado, including power usage, board area usage etc.	4.6800	22.922
Camden	• Got a VM created for our team to work on • In contact with ETG to get licensed software set up • Researched open-sourced RISC-V processors	6	24
John	• Researched FPGAs, RISC-V processors and eINK displays • Work on caravel and efabless	6	24
Levi	• Hardened lab1	6	24
Nicholas	• Work on datapath one and two	6	26

	• Research in open-source RISC-V designs.		

Plans for Upcoming Week

- Calvin:
    - Get rocketchip up and running on the vm
    - Compile and harden the rocketchip default config verilog file
    - Look into isa extension methods and tools, as well as incorporating the rocketchip toolchain
- Camden:
    - Continue with VM setup
        - Get team on board and access to VM
        - Setup software on VM
        - Once everything is set up get it cloned so we can have to VMS
    - Work with team members and finish hardening lab 2 of cpre 381
- John:
    - Continue working with caravel and Efabless
    - Continue research with RISC-V and FPGAs
    - Look into what could help using eINK displays
- Levi:
    - Harden lab1
    - Create guidelines for estimating sizes of things (like 2kb of ram is rougly X mm^2) etc.
- Nicholas:
    - Finish testing and hardening of datapath two
    - Start trying to harden RISC-V processors to see if any issues come up and attempt to address and/or document them.

Summary of weekly advisor meeting

N/A, Professor Duwe had meetings he needed to attend to so we did not have a meeting last week.